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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,923	04/02/2004	Kouji Ogino	D-1609	9423

7590 04/14/2006

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,923	OGINO ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-10 and 12 are rejected under U.S.C. 102(e) as being anticipated by Sueyoshi et al. (US PGPub 2004/0015948 A1).

Claim 1. A control device for controlling an electronic device, comprising:

- connecting means for connecting an external memory, *(Section 1223, lines 1-20 – State the following: "Here, the semiconductor chip 631 corresponds to the semiconductor circuit of the first aspect of the invention, the CPU data bus 640 corresponds to the first transmission line of the first semiconductor circuit, the program module PM_1 corresponds to an instruction for executing a program of the first aspect of the invention, the internal memory 632 corresponds to the storage circuit of the first aspect of the invention, the CPU 637 corresponds to the processing circuit of the first aspect of the*

invention, the switch circuit 633 corresponds to the first connection switching circuit of the first aspect of the invention, the switch circuit 634 corresponds to the second connection switching circuit of the first aspect of the invention, the judgment circuit 635 corresponds to the connection control circuit of the first aspect of the invention, the selection circuit 636 corresponds to the third connection switching circuit of the first aspect of the invention, the external memory 660 corresponds to the storage apparatus of the first aspect of the invention, and the debugger 661 corresponds to the external apparatus of the first aspect of the invention")

- non-volatile storage memory means having a memory region with a portion where data can be electrically rewritten, *(Section 1228, lines 1-5 – State the following: "Above the hardware layer is positioned a communication driver layer. The communication driver layer has positioned in it a communication driver layer for controlling the communication. The program of the communication driver layer is usually stored in a nonvolatile memory")*
- said memory means having a first memory region for storing control program data for operating the electronic device, *(Section 0053, lines 1-7: State the following: Further, the data processing method of the first aspect of the invention preferably further comprises a step of receiving the processing requests from an integrated circuit having a storage unit storage data to be used for processing for a procedure performed with the semiconductor circuit or a communication apparatus inputting and outputting data with the integrated circuit." Section 0054, lines 1-4 – State the following: "A semiconductor circuit of a second aspect of the invention is a semiconductor circuit for processing data in accordance with a plurality of processing requests, comprising an interface for inputting the plurality of processing requests, a storage circuit for storing job management data")*

- a second memory region for storing connection judgment program data to determine whether the external memory means is connected to the connecting means, *(Sections 1210, lines 1-10 and Section 1211, lines 1-8 – State the following: "In this case, the judgment circuit 560 holds the key information K and decryption program 590, accesses the IC card 558 through the CPU data bus 506 and communication circuit 504, reads the fetch access range defining data 584_1, fetch inter-AP call relation defining data 585_1, read access range defining data 584_2, read inter-AP call relation defining data 585_2, write access range defining data 584_3, and write inter-AP call relation defining data 585_3 from the IC card 558, and uses the same decrypted using a predetermined decryption program 590 and key information K. Further, the present invention may store the above decryption program in an encrypted state in the IC card 558, read this through the communication circuit 504 and CPU data bus 506 into the judgment circuit 560, decrypt this by the judgment circuit 560 using predetermined key information, store the decrypted decryption program in the memory 553, and have the judgment circuit 560 read and execute the decryption program from the memory 553")*
- and a third memory region for storing writing program data to rewrite the control program data stored in the first memory region, *(Section 1445, lines 1-6 – Stat the following: "Here, the AP management table data 7300_1, 7300_2, and 7300_3 and the APP table data 7310_1, 7310_2, and 7310_3 are for example preregistered at the time of setup of the SAM chip 708. Further, the AP management table data 7300_1, 7300_2, and 7300_3 and the APP table data 7310_1, 7310_2, and 7310_can be rewritten only by the manager of the SAM chip 708." Section 1488, lines 1-5 – State the following: "the SAM chip 708 has an ASPS communication interface unit 760, external memory communication interface unit 761, bus scramble unit 762, random*

number generation unit 763, encryption/decryption unit 764, storage unit 765, and CPU 766")

- and control means electrically connected to the connecting means and memory means for executing a control program to control an operation of the electronic device, said control means executing the connection judgment program data, and when it is determined that the external memory medium is connected to the control device, the control means executing the writing program data so that at least a portion of the control program data stored in the first memory region of the memory means is rewritten based on external memory medium data stored in the external memory medium. *(Claim 131, lines 1-10 – State the following: "A data processing apparatus comprising: a storage circuit for storing instructions and data of a plurality of programs, a computation circuit for accessing said storage circuit through a transmission line and using the instructions and data of said plurality of programs to execute said plurality of programs, a connection switching circuit interposed between said transmission line and said storage circuit for setting said transmission line and said storage circuit to one of a connection state and disconnection state based on a control signal, a connection control circuit for generating said control signal for control to set said transmission line and said storage circuit to one of a connection state and disconnection state based on access range defining data defining an address range in said storage circuit able to be accessed while said computation circuit is executing said plurality of programs for each of said plurality of programs, an address in said storage circuit for which said computation circuit issues an access request, and executing program instructing information which program in a plurality of programs said computation circuit is executing, and an input/output interface circuit for inputting and outputting data with said computation circuit*

through said transmission line and inputting and outputting data with the outside of that data processing apparatus." Section 1206, lines 1-5 – State the following: "As explained above, the judgment circuit 560 and switch circuit 561 determine the connection state between the memory 553 and CPU data bus 506 based on data defined in advance in accordance with each program in accordance with a program being executed by the CPU 552")

Claim 2. A control device according to claim 1, wherein said control means executes the writing program when data stored in the external memory medium at a predetermined address thereof is read through executing the connection judgment program and the data matches predetermined data stored in the memory means. *(Section 1210, lines 1-10 – State the following: "In this case, the judgment circuit 560 holds the key information K and decryption program 590, accesses the IC card 558 through the CPU data bus 506 and communication circuit 504, reads the fetch access range defining data 584_1, fetch inter-AP call relation defining data 585_1, read access range defining data 584_2, read inter-AP call relation defining data 585_2, write access range defining data 584_3, and write inter-AP call relation defining data 585_3 from the IC card 558, and uses the same decrypted using a predetermined decryption program 590 and key information K")*

Claim 3. A control device according to claim 1, wherein said control means executes operation control program based on the operation control program data stored in the first memory region when data stored in the external memory medium at a predetermined address thereof is read through executing the connection judgment program and the data does not match predetermined data stored in the memory means. *(Sections 1302-1307 – State the following: "Further, the encryption/decryption circuit 6134 decrypts the function module, then judges the legitimacy of the parity data corresponding to that function module. At this time, if judging it*

legitimate, it outputs that decrypted data to the CPU 6137. On the other hand, if judging it is not legitimate, it halts the operation of the CPU 6137 or performs predetermined error processing. Note that, in the present embodiment, the data length of the block data and the data length of the function module may be the same or different. The judgment circuit 6135 generates a judgment result signal S6135 instructing invalidity/disconnection and outputs it to the selection circuit 6136 when the CPU 6137 is accessing (for example, fetching) a confidential program module PM_1. Further, judgment circuit 6135 generates a judgment result signal S6135 instructing validity/connection and outputs it to the selection circuit 6136 when the CPU 6137 is not accessing (for example, fetching) a confidential program module PM_1. The judgment circuit 6135 monitors the addresses and instructions output by the CPU 6137 and flowing over the address bus 6141 and signal line 6142 and, based on the same, judges if the CPU 6137 is accessing the program module PM_1. When the judgment result signal S6135 from the judgment circuit 6135 indicates invalidity/disconnection, the selection circuit 6136 invalidates the HALT signal S6161a input from the debugger 6161 (operation halt request of second aspect of the invention) and does not output it to the CPU 6137. Here, the HALT signal S6161a is a signal instructing to temporarily halt the operation of the CPU 6137.")

Claim 4. A control device according to claim 1, wherein said control means executes the connection judgment program when the control device is turned on. *(Section 1646, lines 7-12 – States the following, in which "running" denotes being "turned on": "These are held in the external memory 707. Therefore, service businesses 715_1 to 715_3 not the developers of the SAM chip 708 can customize their own application programs running on the SAM chip 708 by producing script programs 721_1, 721_2, and 721_3 and downloading them through the SAM chip 708 to the external memory 707")*

Claim 5. A control device according to claim 1, wherein said memory means further includes a fourth memory region for storing compatibility judgment program data for determining whether the external memory medium data stored in the external memory means is compatible and correct, said control means executing the writing program so that at least a portion of the control program data stored in the first memory region in the memory means is rewritten based on the external memory medium data stored in the external memory medium when it is determined that the external memory medium is connected to the control device through executing the connection judgment program and that the external memory medium data stored in the external memory medium is correct through executing the compatibility judgment program. *(Sections 1312-1313 – State the following: "When the judgment result signal S6135 from the judgment circuit 6135 indicates validity/connection, the selection circuit 6136 outputs the CPU internal status read request signal S6161b and CPU internal status rewrite request signal S6161c input from the debugger 6161 to the CPU 6137. Further, the selection circuit 6136 outputs the CPU internal status signal S6137d input from the CPU 6137 in accordance with the CPU internal status read request signal S6161b to the debugger 6161. The CPU 6137 outputs to the address bus 6141 the address of the external memory 6160 and to the signal line 6142 an instruction type instructing signal S6137a showing the type of the instruction being executed and, in accordance with the same, performs processing using instructions and data of the program modules PM_1, PM_2, and PM_3 read from the external memory 6160 through the external data bus 6144 and encryption/decryption circuit 6134")*

Claim 6. A control device according to claim 5, wherein said control means outputs an error signal when it is determined that the external memory medium data stored in the external memory medium is incorrect through executing the compatibility judgment program. *(Section 1302, lines 5-7 – State the*

following: "On the other hand, if judging it is not legitimate, it halts the operation of the CPU 6137 or performs predetermined error processing")

Claim 7. A control device for controlling an operation of an electronic device, comprising:

- non-volatile storage memory means capable of electrically rewriting data stored therein, *(Section 1228, lines 1-5 – State the following: "Above the hardware layer is positioned a communication driver layer. The communication driver layer has positioned in it a communication driver layer for controlling the communication. The program of the communication driver layer is usually stored in a nonvolatile memory")*
- connecting means for connecting an external memory medium to the storage means, *(Section 1223, lines 1-20 – State the following: "Here, the semiconductor chip 631 corresponds to the semiconductor circuit of the first aspect of the invention, the CPU data bus 640 corresponds to the first transmission line of the first semiconductor circuit, the program module PM_1 corresponds to an instruction for executing a program of the first aspect of the invention, the internal memory 632 corresponds to the storage circuit of the first aspect of the invention, the CPU 637 corresponds to the processing circuit of the first aspect of the invention, the switch circuit 633 corresponds to the first connection switching circuit of the first aspect of the invention, the switch circuit 634 corresponds to the second connection switching circuit of the first aspect of the invention, the judgment circuit 635 corresponds to the connection control circuit of the first aspect of the invention, the selection circuit 636 corresponds to the third connection switching circuit of the first aspect of the invention, the external memory 660 corresponds to the storage apparatus of the first aspect of the invention, and the debugger 661 corresponds to the external apparatus of the first aspect of the invention")*

- connection judgment means for determining whether the external memory medium is connected to the memory means with the connection means, *(Sections 1210, lines 1-10 and Section 1211, lines 1-8 – State the following: "In this case, the judgment circuit 560 holds the key information K and decryption program 590, accesses the IC card 558 through the CPU data bus 506 and communication circuit 504, reads the fetch access range defining data 584_1, fetch inter-AP call relation defining data 585_1, read access range defining data 584_2, read inter-AP call relation defining data 585_2, write access range defining data 584_3, and write inter-AP call relation defining data 585_3 from the IC card 558, and uses the same decrypted using a predetermined decryption program 590 and key information K. Further, the present invention may store the above decryption program in an encrypted state in the IC card 558, read this through the communication circuit 504 and CPU data bus 506 into the judgment circuit 560, decrypt this by the judgment circuit 560 using predetermined key information, store the decrypted decryption program in the memory 553, and have the judgment circuit 560 read and execute the decryption program from the memory 553")*
- and writing means for reading external memory medium data stored in the external memory medium when it is determined that the external memory medium is connected to the memory means through executing a connection judgment program, said writing means rewriting at least a portion of operation control program data stored in the memory means based on the external memory medium data read out. *(Claim 131, lines 1-10 – State the following: "A data processing apparatus comprising: a storage circuit for storing instructions and data of a plurality of programs, a computation circuit for accessing said storage circuit through a transmission line and using the instructions and data of said plurality of programs to execute said plurality of programs, a*

connection switching circuit interposed between said transmission line and said storage circuit for setting said transmission line and said storage circuit to one of a connection state and disconnection state based on a control signal, a connection control circuit for generating said control signal for control to set said transmission line and said storage circuit to one of a connection state and disconnection state based on access range defining data defining an address range in said storage circuit able to be accessed while said computation circuit is executing said plurality of programs for each of said plurality of programs, an address in said storage circuit for which said computation circuit issues an access request, and executing program instructing information which program in a plurality of programs said computation circuit is executing, and an input/output interface circuit for inputting and outputting data with said computation circuit through said transmission line and inputting and outputting data with the outside of that data processing apparatus." Section 1206, lines 1-5 – State the following: "As explained above, the judgment circuit 560 and switch circuit 561 determine the connection state between the memory 553 and CPU data bus 506 based on data defined in advance in accordance with each program in accordance with a program being executed by the CPU 552")

Claim 8. A control device according to claim 7, further comprising first judging means for determining whether the writing means rewrites the data stored in the memory means correctly, *(Section 1312, lines 1-9 – State the following: "When the judgment result signal S6135 from the judgment circuit 6135 indicates validity/connection, the selection circuit 6136 outputs the CPU internal status read request signal S6161b and CPU internal status rewrite request signal S6161c input from the debugger 6161 to the CPU 6137. Further, the selection circuit 6136 outputs the CPU internal status signal S6137d input from the CPU 6137 in*

accordance with the CPU internal status read request signal S6161b to the debugger 6161")

- and second judging means for determining whether the writing means completes writing to the memory means normally. *(Section 0940, lines 1-4 – state the following: "The parity processing unit 435 adds parity data to the data to be written in the external memory 407 and verifies the parity data added to data read from the external memory 407")*

Claim 9. A control device according to claim 8, wherein said memory means comprises a first memory region for storing program data, and a second memory region for storing first check data for determining whether the writing means rewrites the data stored in the memory means correctly and for storing second check data for determining whether the writing means completes writing to the memory means normally. *(Section 0027, lines 1-5 – State the following: "A debugger 605 checks the operation of the CPU 602 at the time of development of a program. It uses a HALT signal to temporarily halt the operation of the CPU 602, read internal information of the CPU 602, and inform that information to the program developer")*

Claim 10. A control device according to claim 9, wherein said writing means erases the program data stored in the first memory region after erasing the first check data and the second check data stored in the second memory region, and rewrites the first check data and the second check data to the second memory region in the memory means according to data stored in the external memory medium after writing new program data stored in the external memory medium to the first memory region in the memory means. *(Claim 14, lines 1-4 – State the following: "A semiconductor circuit as set forth in claim 13, wherein said control circuit selects one job management data from said plurality of data modules after updating said status data of said selected job management data")*

Claim 12. A control device according to claim 8, further comprising control means for outputting an error signal when at least one of the first judging means

and the second judging means determines that a result is abnormal, and for controlling the electronic device based on the data rewritten by the writing means when the first judging means and the second judging means determine that the result is normal. *(Section 1302, lines 5-7 – State the following: "On the other hand, if judging it is not legitimate, it halts the operation of the CPU 6137 or performs predetermined error processing")*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C.103(a) as being unpatentable over Sueyoshi et al. as applied to claims 7-8 above.

Sueyoshi teaches the limitations of claims 7-8 for the reasons above.

Sueyoshi's invention differs from the claimed invention in that there is no specific reference to the sequence of steps of judgment.

Sueyoshi fails to teach claim 11, which states "A control device according to claim 8, wherein said first judging means determines whether the writing means rewrites data correctly after the second judging means determines that the writing means completes writing to the memory means normally." However the fact that Sueyoshi does not mention that the steps are done in a particular order does not change the purpose or functionality of the invention. Therefore, it would have been obvious for Sueyoshi's "Data For Processing Method and its Apparatus" to determine whether the writing means rewrites data correctly after the second

judging means determines that the writing means completes writing to the memory means normally, so that the system would run in an efficient and sensible manner.

For further information, please reference Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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